DOMINO Noise Model: A New Crosstalk Noise Model for Dynamic Logic Circuits

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Abstract
DOMINO gates are more vulnerable to crosstalk-induced functional failures compared to static CMOS gates. Previously developed noise models generate pessimistic noise analysis because the effect of keeper in DOMINO is not properly incorporated. In this paper, a new crosstalk noise model is proposed for DOMINO logic gates. Our noise model takes the effect of keeper into account and provides more accurate noise measure. We define the degree of conservatism for noise models and show that our noise model dramatically reduces the pessimism.

I. INTRODUCTION

With the scaling of technology into the nano-meter regime, interconnect delay may limit the performance improvement of a digital circuit [1]. As a practical solution to the problem, the aspect ratio (defined as the interconnect wire thickness divided by the width) of the interconnect is increased [1],[2]. However, this also increases the coupling capacitance between neighboring wires.

Crosstalk noise occurs due to capacitve as well as inductive coupling in a circuit. Inductive coupling becomes significant in global wires at high frequencies [3]. The circuits are prone to failures due to the increase in coupling capacitances between neighboring nets. In this paper, the crosstalk noise as a result of capacitive coupling will be discussed. Crosstalk noise can affect a circuit in two ways – causes glitches and/or changes signal delays. Temporal properties of a circuit can be affected when capacitvely coupled neighboring signals experience simultaneous switching. A number of studies are under way to see the effects of crosstalk noise in timing analysis [4],[5]. A functional failure is possible when an induced noise is propagated and wrongly evaluated at the latch or primary output. Crosstalk-induced glitches can cause severe problems in high-speed circuits for which noise immunity is low. In this paper, we focus on the crosstalk-induced functional failure.

The most accurate and reliable way of checking for circuit failures due to crosstalk is full-scale transistor-level simulation. In [6], Shepard et al. utilize the transistor-level simulations to include the effects of various noise sources. Although this is accurate and realistic, the large overhead in simulation time makes it less appealing for large circuits. An efficient noise model is thus necessary to verify circuits for crosstalk-induced functional failures.

Traditionally, DC noise margin has been preferred for its simplicity. In this analysis, the peak value of the induced noise waveform is compared with the DC noise margin. However, the noise analysis based on DC noise margin is conservative since it does not take into account the temporal property of noise signal. In other words, the peak value of noise can be safely higher than DC noise margin (under certain conditions, such as a very sharp noise spike) without causing any violation at the output. As a result, any noise-avoidance methodology based on DC noise analysis may be very conservative.

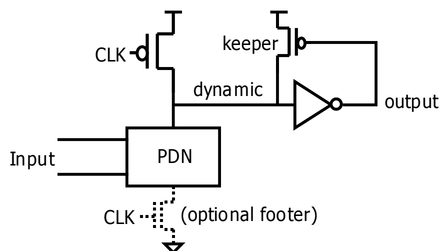


Figure 1 Basic structure of a DOMINO gate

Recently, a dynamic noise model was proposed to compare the noise immunities of different dynamic logic families [7]. Unlike DC noise margin, the dynamic noise margin incorporates the temporal information of noise signals and therefore provides less conservative results. Another methodology was proposed to identify crosstalk-induced failures in DOMINO circuits in [8]. However, these models still produce pessimistic results for DOMINO circuits because the models do not consider the effect of keeper transistor. An analytical noise model for DOMINO was proposed in [9], where transistors are assumed to be operated in subthreshold region. However, this model is not applicable to circuits operated under the condition where the amplitude of crosstalk-induced noise can exceed the threshold voltage of a transistor.

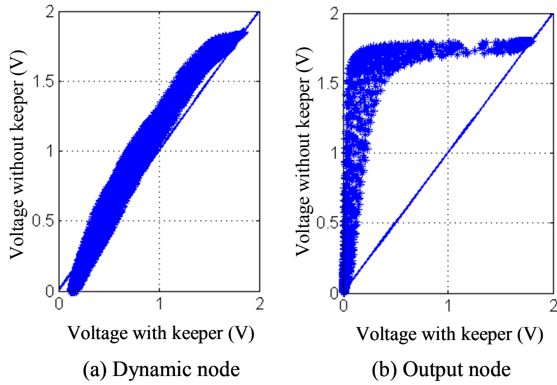
In DOMINO gates, noise immunity is sacrificed for high performance. The DC noise margin of DOMINO gates is equal to the threshold voltage of pull-down transistors. Unlike static CMOS gates, the charge lost from dynamic node due to noise cannot be restored in DOMINO gates. This makes DOMINO gates more vulnerable to noise than static CMOS gates. A keeper is used to restore any loss of charge from the dynamic node. In this paper, we propose a new analytical crosstalk noise model for DOMINO gates in which the effect of keeper is incorporated. We compare different noise models in terms of the degree of conservatism.

II. DOMINO Logic Gates

Figure 1 shows the general structure of DOMINO gates. The input of the inverter (the output of the dynamic gate) is defined as the dynamic node. The charge at the dynamic node is very important for determining the functional behavior of the output node.

The operation of DOMINO gates can be divided into two regions; precharge and evaluation. During the precharge period, the dynamic node is charged to a 'high' value. Any noise at the input nodes during the precharge period can be safely ignored. When the clock signal goes 'high', the evaluation period begins. During the evaluation period, an induced noise at the input can affect the gate functionality.

The keeper PMOS transistor alleviates the charge-sharing effect. It also helps to prevent the propagation of noise from input to the output. To verify this, simple experiments were performed with a precharged-high single-input DOMINO gate. 4500 different shapes of noise pulses were applied at the input during the evaluation period and the voltage deviations were measured at the dynamic node as well as at the output node of a DOMINO gate. The scatter plot in Figure 2(a) compares the voltage deviations measured at the dynamic node with and without the keeper. Any point above the solid line in the figure indicates that the voltage deviation with keeper is smaller than without keeper, which means a gate with



(a) Dynamic node (b) Output node

Figure 2 Keeper effect on noise immunity

keeper is more immune to coupling noise. It can be seen from the figure that for some noise inputs, the voltage deviation at the dynamic node is larger with keeper than the deviation without keeper (the points below the solid line). This is because for a small input noise the coupling between input and dynamic node dominates the voltage deviation at the dynamic node. Therefore, for a small input noise, the dynamic node follows the input voltage change when there is no keeper. With the presence of a keeper, however, this effect is smaller due to the increase in parasitic capacitance at the dynamic node.

The effect of keeper in noise immunity is more clearly observed at the output node. Figure 2(b) compares the voltage deviations measured at the output node for different noise inputs. It is observed that the voltage deviation at the output is much larger when there is no keeper (area above the solid line).

It is clear from the above experiments that a realistic noise model for DOMINO logic should incorporate the effect of keeper. The noise model proposed in [7] is not appropriate for DOMINO gates since it cannot handle the keeper effect. In the next subsection, we explain the proposed DOMINO noise model.

III. Noise model for DOMINO gates

Figure 3 describes the noise model for DOMINO gates. We denote the signal of interest as victim (input of PDN) and the signal affecting the victim as aggressor. During the evaluation period, input signal either stays at 'low' or switches from 'low to high'. The victim is vulnerable to crosstalk noise when it stays at 'low'. Due to an aggressor switching, noise can be induced on a victim net through capacitive coupling. The number of aggressors coupled to a victim net can be more than one. However, this does not affect our model since we assume that the induced noise waveform at the input is readily available via transistor-level simulation or analytical model. The failure due to crosstalk noise at input for DOMINO gate is defined as follows[1];

- *Failure occurs in a DOMINO gate when the voltage deviation at dynamic node exceeds DC noise margin of the following inverter.*

A. DOMINO noise margin

In order to obtain an analytical solution for noise margin for DOMINO gates, let us consider the current model for the PDN NMOS transistor. The transistors in deep-submicron technology

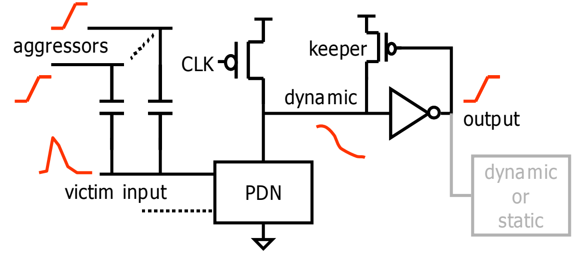


Figure 3 Crosstalk noise model for DOMINO gates

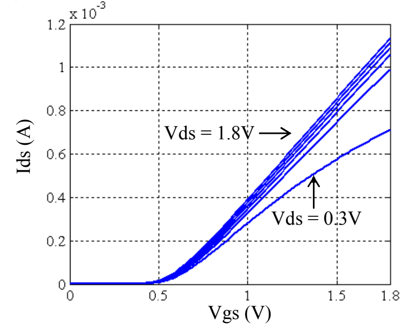


Figure 4 Drain-to-source current vs. gate voltage (NMOS)

experience short-channel effects [10]. As a result, there exists a linear relationship between drain-to-source current and gate voltage for a certain range of drain-to-source bias. This is depicted in Figure 4 for an NMOS transistor (width=1.8um) with 180nm technology and 1.8V supply voltage. The curve at the bottom corresponds to V_{ds}=0.3V. The rest of the curves are for the successive increase of V_{ds} by 0.3V. As it can be seen from the figure, except for the small bias between drain and source, it is acceptable to model the current as a linear function of gate (input) voltage.

Therefore, the current flowing from the dynamic node can be expressed as

$$i_d(t) = g_m \times (v_{in}(t) - V_{th}) \tag{1}$$

where i_d is the current at dynamic node, v_{in} is the input noise voltage, V_{th} is the threshold voltage of PDN and g_m (di_{ds}/dv_{gs}) is the transconductance of PDN. We calculate g_m considering $V_{ds}=V_{dd}$.

The voltage deviation at the dynamic node is determined by the capacitance at the node and the amount of charge lost due to noise activity. The voltage deviation, V_d, at the dynamic node can be obtained as follows:

$$\begin{aligned} Q_d &= \int_T i_d(t)dt = \int_T g_m \times (v_{in}(t) - V_{th})dt \\ V_d &= \frac{Q_d}{C_d} = \frac{\int_T g_m \times (v_{in}(t) - V_{th})dt}{C_d} \end{aligned} \tag{2}$$

where Q_d is the amount of charge lost from dynamic node and C_d is the total capacitance at the node including all the parasitic and wire capacitances. Integration is performed for the time period T, for which the input noise $v_{in}(t)$ is larger than V_{th}. By comparing V_d with the DC noise margin of the inverter, NM_{inv}, we determine if a gate will have a failure. The DC noise margin is obtained from voltage transfer characteristic at unity gain point.

[1] This concept of failure is similar to the one proposed in [7].

Depending on the voltage change at the dynamic node, a current flows through the keeper supplying a certain amount of charge to the dynamic node. Therefore, the actual loss of charge, Q_{d_new}, from the dynamic node can be modified as follows

$$Q_{d_new} = Q_d - Q_{keep}$$

where Q_{keep} is the amount of charge supplied by keeper. The voltage deviation at the dynamic node then can be rewritten as

$$V_d = \frac{Q_{d_new}}{C_d} = \frac{\int_T g_m \times (v_{in}(t) - V_{th})dt - Q_{keep}}{C_d} \quad (3)$$

Q_{keep} can be obtained by integrating the current flowing through keeper with respect to time. However, it is very difficult to analytically model the keeper current since the gate of keeper PMOS is connected to the output node. We simplify this problem by cutting off the feedback and connecting the gate of keeper to ground. This might appear as an overestimation of keeper current. However, the gate voltage of the keeper remains close to zero due to the high gain of the inverter until the voltage deviation at the dynamic node crosses the trip point of the inverter. Once the voltage deviation exceeds the trip point, the inverter switches causing a failure at the output. Also note that the trip point of the inverter is close to V_{dd} for faster operation of the dynamic circuit and hence, the keeper is almost fully turned on until the inverter switches. Therefore, the simplification made in our model (connecting the gate of the keeper to ground) does not introduce a significant error in estimating the keeper current.

The transient behavior of current flowing through the keeper is modeled as a triangular waveform as shown in Figure 5. The peak current, I_{k_max}, is obtained assuming the maximum voltage deviation at the dynamic node equal to NM_{inv} (the condition for functional failure). The duration of keeper current is equal to T, for which the input noise is greater than V_{th} of PDN NMOS (Figure 5). The charge supplied by the keeper is obtained by integrating the transient current during T. However, the actual duration of the keeper current waveform is longer than T because of the feedback mechanism. This makes our model conservative enough not to underestimate the effect of crosstalk noise.

Finally, incorporating keeper charge into eq.(3), we get;

$$V_d = \frac{\int_T g_m \cdot (v_{in}(t) - V_{th})dt - \left|\frac{1}{2} \cdot T \cdot I_{k_max}\right|}{C_d} \quad (4)$$

According to the definition of the failure, V_d has to be larger than the DC noise margin of the inverter. Equating V_d to NM_{inv} in eq.(4) we get

$$\int_T (v_{in}(t) - V_{th})dt = \frac{NM_{inv} \cdot C_d + \left|\frac{1}{2} \cdot T \cdot I_{k_max}\right|}{g_m}$$

We define the DOMINO noise margin as

$$DNM_{DOMINO} = \frac{NM_{inv} \cdot C_d + \left|\frac{1}{2} \cdot T \cdot I_{k_max}\right|}{g_m} \quad (5)$$

DNM_{DOMINO} has the unit of volt.sec and is compared with time-integration of input noise to verify functional failure. Note that the keeper effect does not contribute to any extra computational cost since T is obtained from the already available input noise pulse. I_{k_max} can also be pre-characterized. Also note that neglecting the keeper effect, DOMINO noise margin reduces to dynamic noise margin proposed in [7].

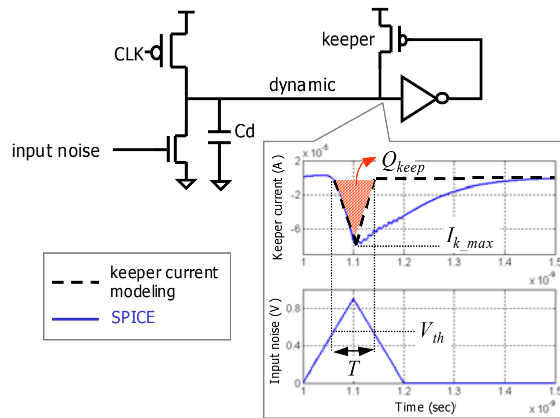


Figure 5 Estimation of keeper charge

IV. Comparison of various noise models

In this section, DOMINO noise margin is verified through SPICE simulation. Our noise model is also compared with different noise models in terms of its degree of conservatism as defined in the following subsection B.

A. Experimental setup

We verified our noise model for DOMINO gates with 180nm technology and with the supply voltage equal to 1.8V. We used DOMINO inverter in our experiments because it reflects the property of DOMINO OR gates which are most sensitive to coupling noise. To account for the possible combinations of input noise, 4500 different noise pulses were generated. These noise pulses had triangular shapes with different heights and widths. The transconductance g_m for PDN NMOS was obtained from BSIM3 current model. The DC current flowing through the keeper with drain-to-source bias equal to (NM_{inv}-V_{dd}) was also obtained using BSIM3 current model. These current values and g_m were pre-characterized for different PMOS and NMOS widths, respectively.

B. Conservatism of different noise models

For a large number of different input noise pulses, a gate was verified with three different noise models:

- *DC noise model (DC NM): The peak value of input noise is compared with the DC noise margin, i.e. V_{th} of PDN NMOS.*
- *Dynamic noise model (DNM)[7]: The time-integration of input noise, $\int_T (v_{in}(t) - V_{th})dt$, is compared with dynamic noise margin.*
- *DOMINO noise model: $\int_T (v_{in}(t) - V_{th})dt$ is compared with DOMINO noise margin obtained from eq.(5).*

We define the "true violation" as follows;

- *Violation occurs when the gate output switches due to a noise coupled at its input.*

A complete switching of a signal at the output does not necessarily mean the functional failure of a circuit. It depends on the sensitization condition of the path through which the noise is propagated to the latch or the primary output. However, we restrict our attention to local violation of a logic value.

We also define the degree of conservatism based on the experimental results as follows.

- *The percentage degree of conservatism is defined as 100·(x-y)/y, where x is the number of violations identified by a noise model and y is the number of true violations. If a model is perfect, it will have zero degree of conservatism.*

DOMINO gates with different sizes of equivalent PDN NMOS are verified. The histogram in Figure 6 shows the number of violations identified using different noise models along with the number of true violations. Horizontal axis represents the width of NMOS transistor of PDN. It can be seen from the figure that by using DOMINO noise margin we can reduce the conservatism compared to DC NM and DNM analysis. It is also observed that all true violations are covered by the three different noise models. In terms of the degree of conservatism, DOMINO noise model shows an improvement up to 72% over DC noise model and up to 10% over dynamic noise model.

It is also observed that the degree of conservatism of a noise model does not vary significantly for different PDN widths. This is because the width of keeper PMOS and the skew of inverter are changed proportionally with the size of PDN NMOS. As a result, the increase in the PDN widths does not affect the noise margin, or noise immunities.

C. Noise immunity vs. performance

In order to improve the noise immunity, the width of keeper PMOS transistor can be increased. However, increasing keeper size degrades the performance of the gate. Changing the skew of the inverter would also result in a similar effect. To observe the effect of keeper size in different noise models, we repeated the experiments with different widths of the keeper while keeping the widths of other transistors unchanged. Simulation results are summarized in Table 1 for different keeper sizes as a fraction of PDN NMOS widths. The number of violations (#viol) and the corresponding degree of conservatism (%con) are tabulated for different noise models. The last row shows the number of true violations. The decrease in the number of true violations implies that noise immunity improves as keeper size increases. Note that as the keeper size increases, the number of violations based on DOMINO noise model decreases much faster than dynamic noise model based analysis. This is because in DOMINO noise model analysis, the effect of keeper on noise immunity is directly taken into account while in dynamic noise model based analysis, the number of violations slightly reduces only due to the increase in parasitic capacitance at the dynamic node. However, the degree of conservatism in DOMINO noise analysis increases with keeper size because the error in estimating the amount of charge supplied by the keeper increases with keeper size.

The noise immunity can be traded for improved performance in

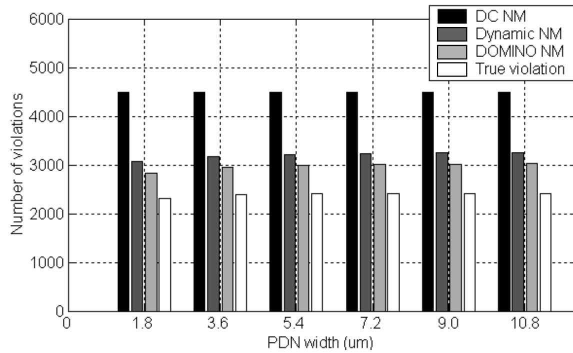


Figure 6 Number of violations for different noise models

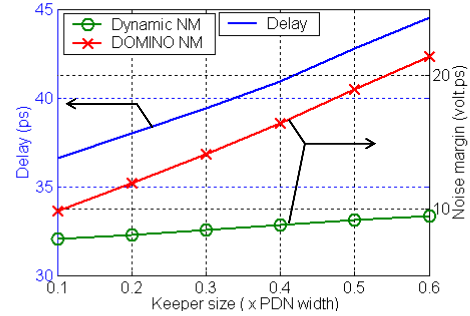


Figure 7 Noise immunity vs. performance

DOMINO logic gates. Figure 7 shows the variation in delay, dynamic noise margin and DOMINO noise margin for different keeper sizes. Delay is measured from input to output at 50% of V_{dd} for a ramp input. It can be seen from the figure that both delay and DOMINO noise margin increase with keeper size. However, dynamic noise margin does not show much variation. The slight increase in dynamic noise margin is due to the increase in the parasitic capacitance at the dynamic node.

V. Conclusions

We proposed a DOMINO noise model and a DOMINO noise margin to verify crosstalk-induced functional failures in DOMINO logic circuits. The proposed noise model is able to cover all true violations caused by crosstalk noise. By properly modeling the effect of keeper, it is shown that our noise model provides less pessimistic results compared to conventional DC noise analysis and dynamic noise analysis.

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Table 1 Comparison of different noise models

keeper size		0.1x	0.2x	0.3x	0.4x	0.5x	0.6x
DC NM	#viol	4500	4500	4500	4500	4500	4500
	%con	72.67	88.52	107.0	129.9	160.1	196.2
Dynamic NM	#viol	3204	3168	3129	3098	3066	3031
	%con	22.94	32.72	43.93	58.30	77.23	99.54
DOMINO NM	#viol	3092	2949	2804	2638	2464	2285
	%con	18.64	23.54	28.98	34.80	42.43	50.43
No. of true violation		2606	2387	2174	1957	1730	1519