IMPACT Multicore Prototyping Environment

Future processing environments are expected to be based in large part on microprocessor components containing significant numbers of processor cores, ranging from dozens to hundreds. Realization of the potential of such systems presents profound software challenges for a number of reasons. Conventional HPC parallelization techniques are not expected to find much utility: the applications are not typical of scientific codes, but instead more closely represent tasks more akin to embedded devices: media processing, interactive and graphical applications, upgraded legacy programs, etc. The expected high-bandwidth memory and interconnect structure, in fact, is more likely to respond to advanced compilation techniques.

Many such techniques are found in the rapidly evolving IMPACT compiler, which produced seminal papers on the "superblock" and "hyperblock" structures. The IMPACT compiler is now being transformed into a strong compiler environment for the multi-core chips. However, producing a functional, high-performance compiler for advanced multi-core chips is a daunting, complex, and challenging task, made all the more difficult by the fact the hardware is several years away from production status, such as the recently announced Intel Terascale processor with 80 cores. High density soft core emulation environments, as represented by the BEE2 board, offer a compelling platform for the IMPACT work. Furthermore, the expertise already developed at Illinois in embedded and mainstream Linux on FPGAs provides additional synergy for rapid deployment of the proposed multi-core compilation techniques. It is our assertion that not only will acquisition of a number of BEE2 boards greatly accelerate the actual compiler development into this area, but that GSRC collaborators at other sites will derive immediate and ongoing benefits by direct and early application of compiler, OS, and locally produced IP on a common platform.

This request proposes for Phase One, the immediate acquisition of two self-contained chassis: one for stable execution of compiled code, and a second for new development platform in which frequent downtime may occur due to OS and hardware work. “New development in this context is meant to include research development of other projects at Illinois, for example, distributed deployment of the Reliability and Security Engine under development in the Resilient Theme; prototyping components of self-assembling structures of networked entities for the Alternative Theme. The hardware will be online and available to all GSRC researchers at Illinois, and possibly other more distant sites, network permitting. If the approach proves valuable, a third Phase One device may be requested in 1Q07. Phase two hardware will be an additional three units, a second production unit to extend the capability to in excess of 512 processor chip emulation, a remote site to permit concurrent development and cross-validation, and a third expressly devoted to operating system development. We propose that initiation of phase two be based upon the level of success of the two initial board, probably reviewed at the September 2007 GSRC annual meeting. A tentative timeline anticipates delivery of functional BEE2 systems in January 2007, tentative first code compilation in 6 months, and early applications in an additional 3 months. Given the aggressive timeline, early hardware availability is a critical component of any successful effort.