

# **Fault Emulation Using the BEE2 Board**

Tim Cheng

University of California, Santa Barbara

October 29, 2006

We plan to develop a fault emulation engine using the BEE2 board. Fault simulation is a fundamental tool in test evaluation and would be used widely and repeated for several research tasks in the GSRC reliability theme. However, fault simulation remains a very time consuming task due to the high fault count needed for simulation and its slow underlying software. The real-time simulation capability of a hardware emulator offers the promise of significant performance improvement for this task. An efficient fault emulator can also be used as an evaluation platform for better understanding the behaviors of various new fault models.

We will employ a serial fault emulation algorithm for the initial implementation. For simulating a large number of faults, however, the need to reconfigure the system for each of the injected faults could result in prohibitively high reconfiguration time, which would be a bottleneck in the entire fault emulation process. We will investigate adding additional circuitry to the emulated design which enables the injection of a large number of faults for each FPGA configuration, while still allowing emulation of each fault sequentially without reconfiguration. After the initial implementation of a serial fault emulator, we will enhance the process by incorporating some ideas used in software fault simulation for further performance improvement.

We plan to use some existing modules/designs already implemented in BEE2 as the design drivers for the fault emulator implementation. We will demonstrate the fault emulation system for stuck-at faults and bridging faults with a performance at least four to five orders of magnitude faster than the existing software fault simulation tools by August 31, 2007.

After the emulator is implemented, we will continue to use the BEE2 board for our research in the reliability theme. Specifically, we plan to exam the feasibility of using the BEE2 board to demonstrate self-recovery for re-configurable systems. To mimic error occurrence, we would randomly inject faults into the design implemented in the BEE2 board. The embedded self-test and diagnosis implemented in the design would then automatically detect the faults and identify the defective blocks. Such information would then trigger reconfiguration to replace the defective blocks for error recovery. This task will take longer for completion and will be done after the research on error recovery mechanism is completed. We estimate that a demo of error recovery using the BEE2 board would be done by August 31, 2008.